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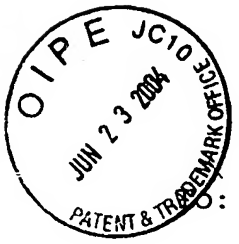
NUS-03-001



June 14, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/802,563 03/17/04

Hong Yu Yu et al.

A THERMAL ROBUST SEMICONDUCTOR DEVICE USING HFN AS METAL GATE ELECTRODE AND THE MANUFACTURING PROCESS THEREOF

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 21, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 6/21/04

Heuss et al. in his abstract, Abstract C7.6 "Thermal Stability of Hafnium and Hafnium Nitride (HfNx) Gate Electrodes on Silicon Dioxide," pp. 67, 76-77, Materials Research Society Proceedings, April 2000, discusses the use of HfNx as the metal gate material but does not recommend the applicaton of HfN as the gate electrode.

While refractory metal nitrides such as TaN and TiN have been extensively investigated as the potential solutions to replace poly-Si, these materials show liminted thermal stability and thus are incompatible with conventional CMOS processes (with thermal processing for activating the source and drain regions). See "Physical and Electrical Properties of Metal Gate Electrodes on HfO2 Gate Dielectrics," by J.K. Schaeffer et al., Journal of Vacuum Science and Technology, Vol. 21(1), Jan/Feb. 2003, pp. 11-17, and "Thermal Stability of PVD TiN Gate and Its Impacts on Characteristics of CMOS Transistors," by M. Wang et al., 6th International Symposium on Plasma Process Induced Damage, May 14-15, Monterey Ca USA, 2001, pp. 36-39.

U.S. Patent 6,511,911 to Besser et al., "Metal Gate Stack with Etch Stop Layer," gives a metal gate stack structure comprised of Tungsten, tantalum, TiN and etch stopper which is used for the deep submicron CMOS process.

U.S. Patent 6,383,879 to Kizilyalli et al., "Semiconductor Device Having a Metal Gate with a Work Function Compatible with a Semiconductor Device," presents a method to form dual metal gates for the different work function for NMOS and PMOS transistors.

The thermal stability of HfN is superior to TiN and TaN, due to its negatively larger heat of formation coompared to that of TiN and TaN (HfN:-88.2, TiN:-80.4, TaN:-60.3, kcal/mol). See "Properties and Microelectronic Applications of Thin Films of Refractory Metal Nitrides," by M. Wittmer, Journal of Vacuum Science Technology A, vol. 3, pp. 1797-1803.

"Metal Gates for Advanced Sub-80-nm SOI CMOS Technology," by B. Cheng et al., 2001 IEEE International SOI Conference, 10/01, pp. 91-92, investigates the impact of the gate work function on PD and FD SOI current drive and short-channel performance.

U.S. Patent Application Publication US 2003/0197230 A1 to Mocuta et al., "High Performance CMOS Device Structure with Mid-Gap Metal Gate," discloses high performance (surface channel) CMOS devices with a mid-gap work function metal gate.

U.S. Patent 6,225,168 to Gardner et al., "Semiconductor Device Having Metal Gate Electrode and Titanium or Tantalum Nitride Gate Dielectric Barrier Layer and Process of Fabrication Thereof," discloses a metal gate electrode and a titanium or tantalum nitride as gate dielectric barrier layer and the processes for fabricating such devices.

U.S. Patent 6,617,624 to Powell, "Metal Gate Electrode Stack with a Passivating Metal Nitride Layer," teaches a metal gate stack including a doped polysilicon, TiN and Tungsten with Nitride passivation and its formation processes.

U.S. Patent 6,043,157 to Gardner et al., "Semiconductor Device Having Dual Gate Electrode Material and Process of Fabrication Thereof," discloses a process for forming dual gates where one gate is polysilicon and the other gate is metal.

U.S. Patent 5,960,270 to Misra et al., "Method for Forming a MOS Transistor Having a Metallic Gate Electrode that is Formed After the Formation of Self-Aligned Source and Drain Regions," discloses a process wherein the same mid-gap work function metal is used for both n- and p-gates.

U.S. Patent 6,083,836 to Rodder, "Transistors with Substitutionally Formed Gate Structures and Method," teaches a dummy gate process where two gates are formed.

U.S. Patent 6,576,937 to Schaeffer, III et al., "Semiconductor Structure and Process for Forming a Metal Oxynitride Dielectric Layer," discloses a semiconductor device and the process of forming a metal oxy-nitride gate dielectric layer or a metal-silicon oxy-nitride gate dielectric layer.

U.S. Patent 6,479,362 to Cunningham, "Semiconductor Device with High-Temperature-Stable Gate Electrode for Sub-Micron Applications and Fabrication Thereof," discusses an improved process for high-performance sub-micron CMOS technologies as may be found in high-performance logic applications such as state-of-the-art microprocessors or embedded DRAM implementations.

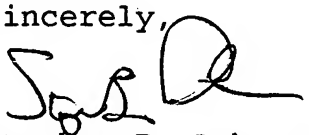
U.S. Patent 6,208,004 to Cunningham, "Semiconductor Device with High Temperature-Stable Gate Electrode for Sub-Micron Applicatons and Fabrication Thereof," discusses an improved process for high-performance sub-micron CMOS technologies as may be found in high-performance logic applications such as state-of-the-art microprocessors or embedded DRAM implementations.

U.S. Patent Application Publication US 2002/0037615 A1 to Matsuo, "Semiconductor Device and Method of Fabricating the Same," discusses an improvement of gate electrodes on an n-type MIS transistor and a p-type MIS transistor.

U.S. Patent 6,051,487 to Gardner et al., "Semiconductor Device Fabrication Using a Sacrificial Plug for Defining a Region for a Gate Electrode," teaches a dummy gate process using a polysilicon or a metal gate.

"International Technology Roadmap for Semiconductor," Semiconductor Industry Association, San Jose, CA (ITRS-2001), (we were only able to get the updated 2003 version, a copy of which is included for reference), discusses using metal gate in CMOS devices which can alleviate the problem caused by poly silicon gate associated depletion effects and dopant penetration effects.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
NUS-03-001	10/802,563
Applicant: Hong Yu Yu et al.	
Filing Date: 03/17/04	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6225168	5/1/01	Gardner et al.	438	287	6/4/98
	6383879	5/7/02	Kizilyalli et al.	438	303	5/17/00
	6511911	1/28/03	Besser et al.	438	656	4/3/01
	6617624	9/9/03	Powell	257	288	3/15/01
	6043157	3/28/00	Gardner et al.	438	692	12/18/97
	5960270	9/28/99	Misra et al.	438	197	8/11/97
	6083836	7/4/00	Rodder	438	690	12/18/98
	6576967	6/10/03	Schaeffer, III et al.	257	411	9/18/00
	6479362	11/12/02	Cunningham	438	369	2/14/01
	6208004	3/27/01	Cunningham	257	413	8/19/98
	6051487	4/18/00	Gardner et al.	438	585	12/18/97

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- Heuss et al., Abstract C7.6 "Thermal Stability of Hafnium and Hafnium Nitride (HfN_x) Gate Electrodes on Silicon Dioxide," pp. 67, 76-77, Materials Res. Soc. Proc., April 2000.
- "Physical and Electrical Properties of Metal Gate Electrodes on HfO_2 Gate Dielectrics," by J.K. Schaeffer et al., Journal of Vacuum Science and Tech., Vol. 21(1), Jan/Feb. 2003, pp. 11-17.

EXAMINER	DATE CONSIDERED

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

- "Thermal Stability of PVD TiN Gate and Its Impacts on Characteristics of CMOS Transistors," by M. Wang et al., 6th Int'l Symp. on Plasma Process Induced Damage, May 14-15, 2001, Monterey, CA, USA, pp. 36-39.
- "Metal Gates for Advanced Sub-80-nm SOI CMOS Technology," by B. Cheng et al., 2001 IEEE Int'l SOI Conf., 10/01, pp. 91-92.

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

- "Properties and Microelectronic Applications of Thin Films of Refractory Metal Nitrides", by M. Wittmer, Jrnl. of Vacuum Science Tech. A, Vol. 3, pp. 1797-1803,
- "Int'l Tech. Roadmap for Semiconductor", Semiconductor Industry Association, San Jose, CA (ITRS-2003).

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

–	US Patent App. Pub. US 2003/0197230 A1 to Mocuta et al., Pub. Date 10/23/03, Filed 04/19/02, US Class 257/407.
–	US Patent App. Pub. US 2002/0037615 A1 to Matsuo, Pub. Date 03/28/02, Filed 09/25/01, US Class 438/241.

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